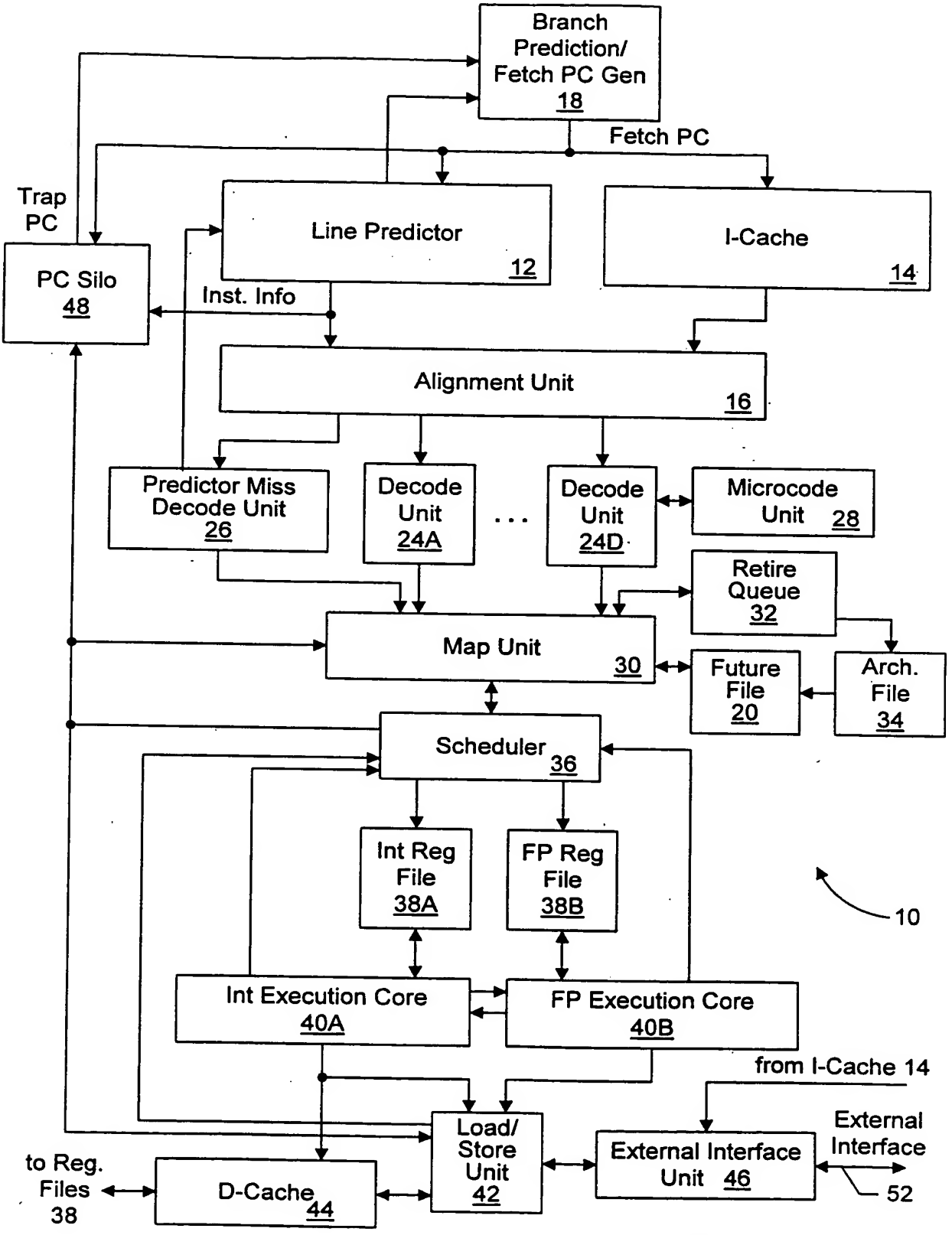
Branch Prediction/ Fetch PC Gen 18
Fetch PC
Trap PC
Line Predictor 12
I-Cache 14
PC Silo 48
Inst. Info
Alignment Unit 16
Predictor Miss Decode Unit 26
Decode Unit 24A
Decode Unit 24D
Microcode Unit 28
Retire Queue 32
Map Unit 30
Future File 20
Arch. File 34
Scheduler 36
Int Reg File 38A
FP Reg File 38B
10
Int Execution Core 40A
FP Execution Core 40B
from I-Cache 14
Load/ Store Unit 42
External Interface Unit 46
External Interface
52
to Reg. Files 38
D-Cache 44

FIG. 1

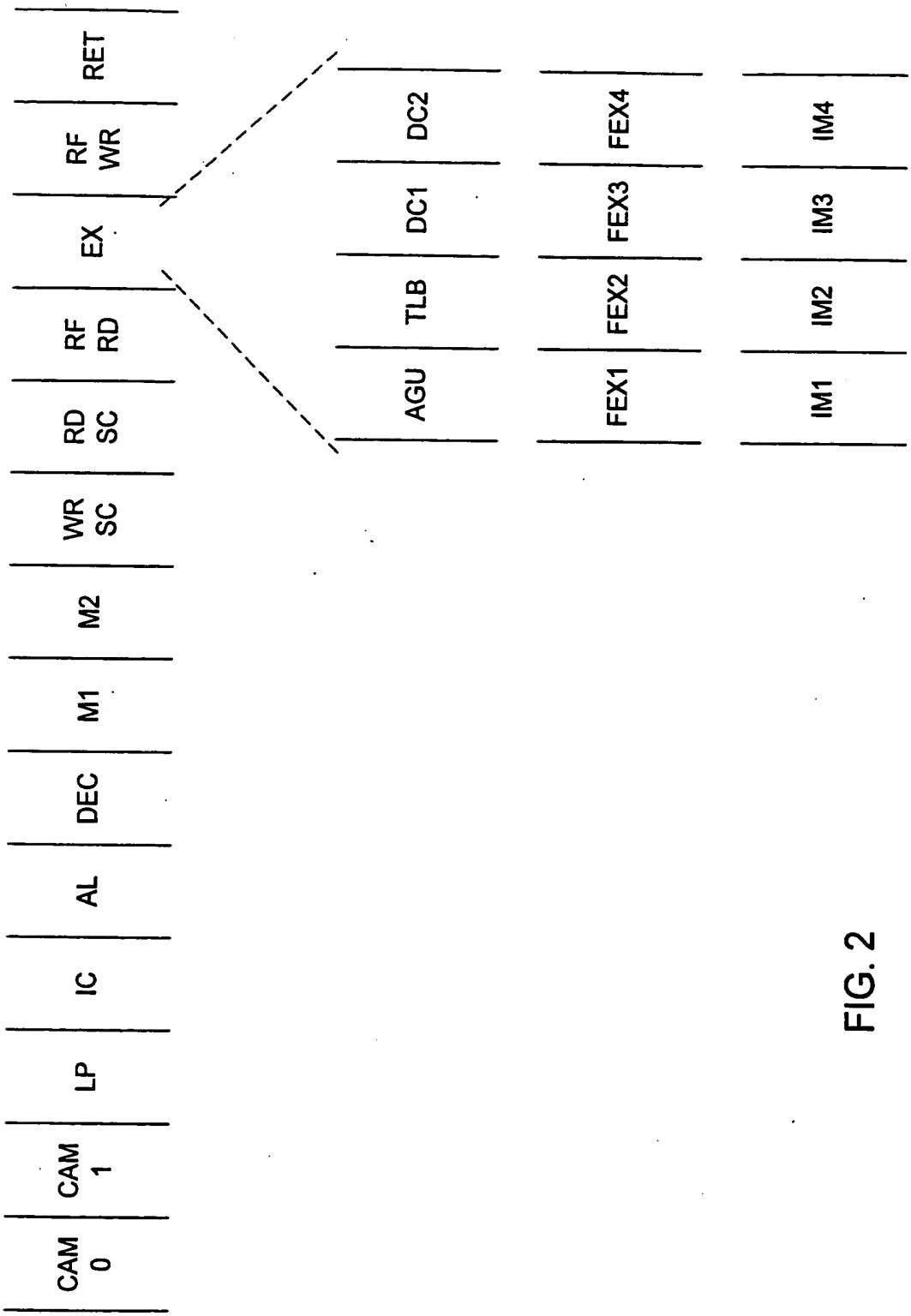
CAM 0
CAM 1
LP
IC
AL
DEC
M1
M2
WR SC
RD SC
RF RD
EX
RF WR
RET
AGU
TLB
DC1
DC2
FEX1
FEX2
FEX3
FEX4
IM1
IM2
IM3
IM4

FIG. 2

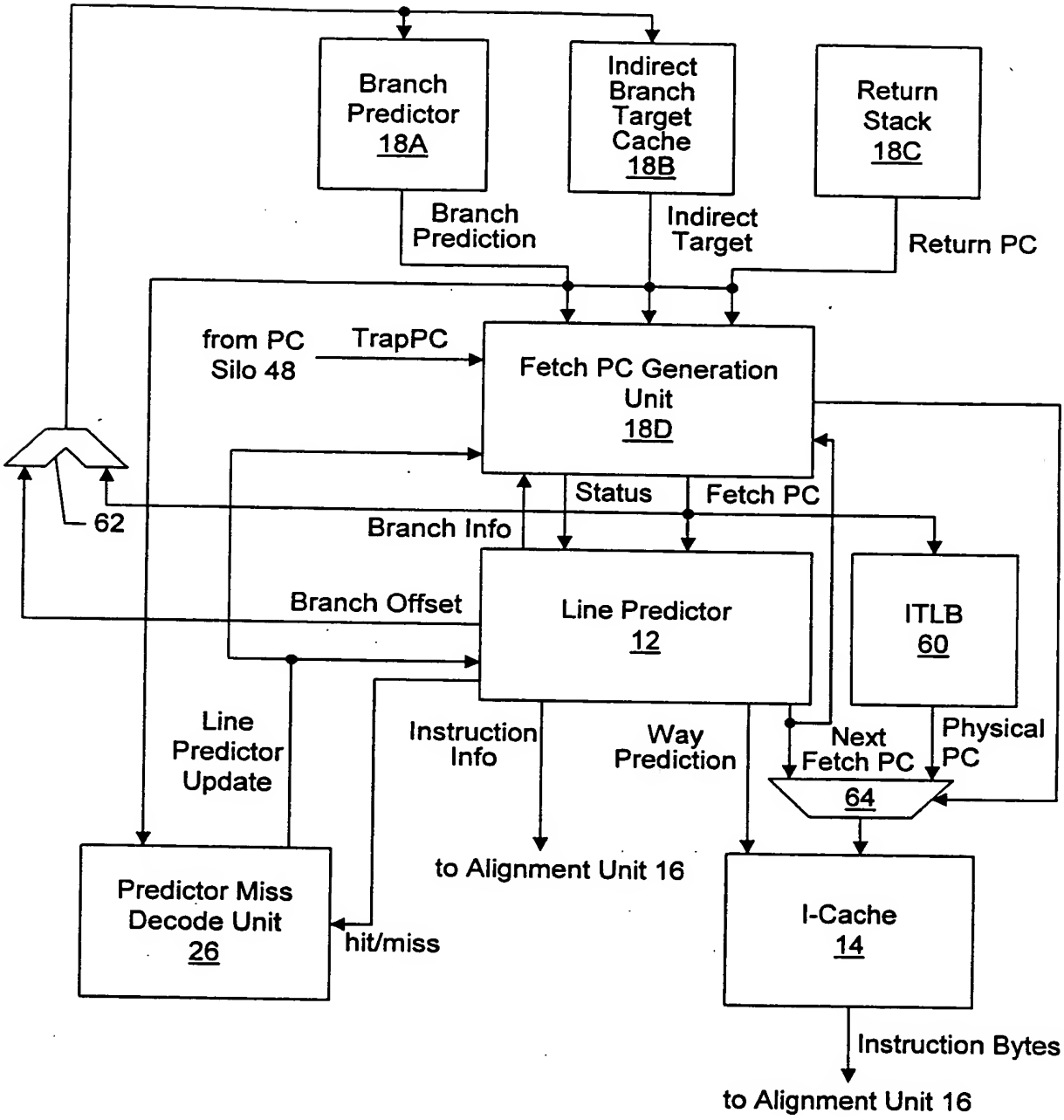
Branch Predictor 18A
Indirect Branch Target Cache 18B
Return Stack 18C
Branch Prediction
Indirect Target
Return PC
from PC Silo 48
TrapPC
Fetch PC Generation Unit 18D
62
Status
Fetch PC
Branch Info
Branch Offset
Line Predictor 12
ITLB 60
Line Predictor Update
Instruction Info
Way Prediction
Next Fetch PC
Physical PC
64
to Alignment Unit 16
Predictor Miss Decode Unit 26
hit/miss
I-Cache 14
Instruction Bytes
to Alignment Unit 16

FIG. 3

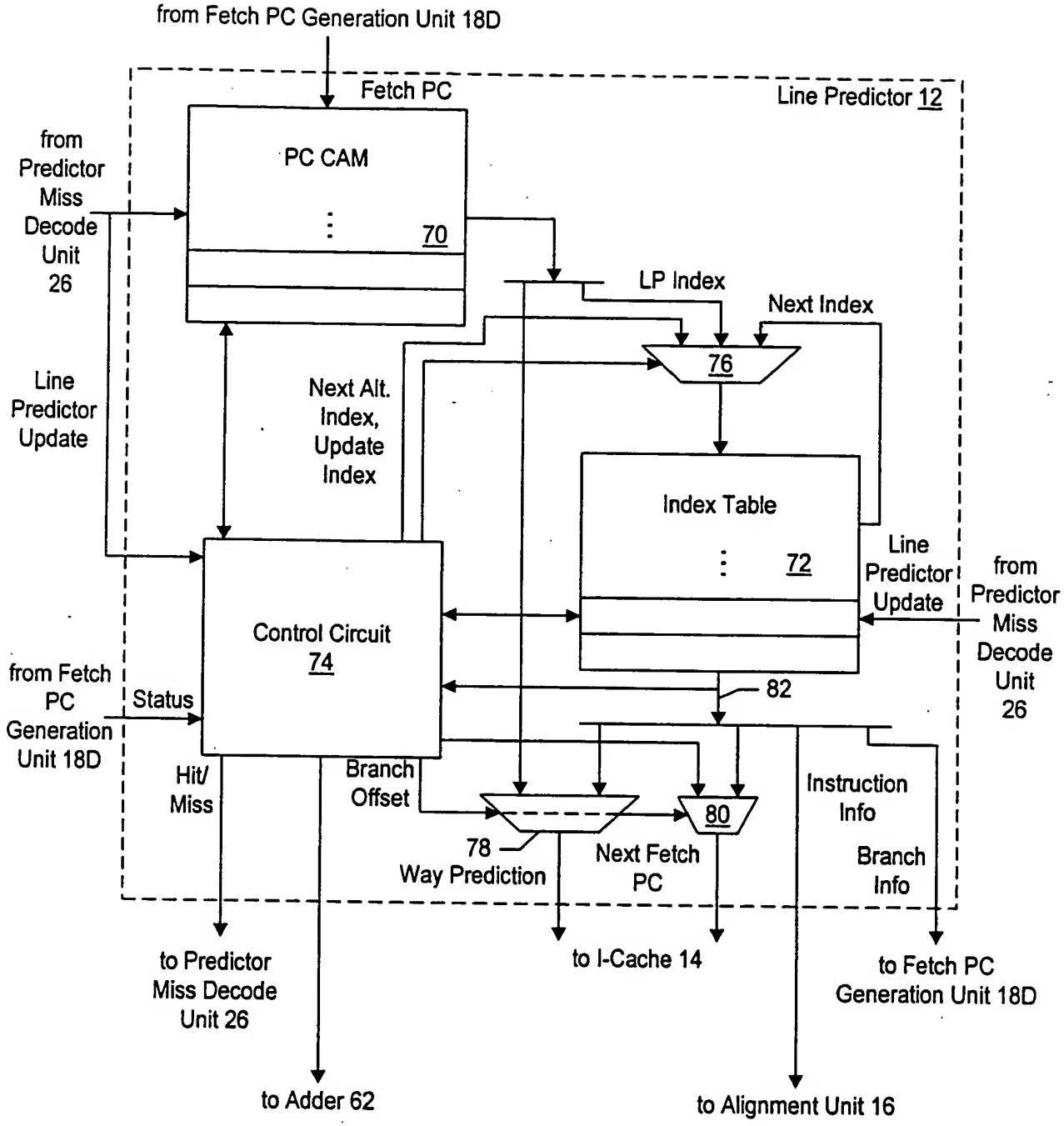
from Fetch PC Generation Unit 18D
Fetch PC
Line Predictor 12
from Predictor Miss Decode Unit 26
PC CAM
70
LP Index
Next Index
76
Line Predictor Update
Next Alt. Index, Update Index
Index Table
72
Line Predictor Update
from Predictor Miss Decode Unit 26
Control Circuit 74
from Fetch PC Generation Unit 18D
Status
82
Hit/ Miss
Branch Offset
80
Instruction Info
78
Way Prediction
Next Fetch PC
Branch Info
to Predictor Miss Decode Unit 26
to I-Cache 14
to Fetch PC Generation Unit 18D
to Adder 62
to Alignment Unit 16

FIG. 4

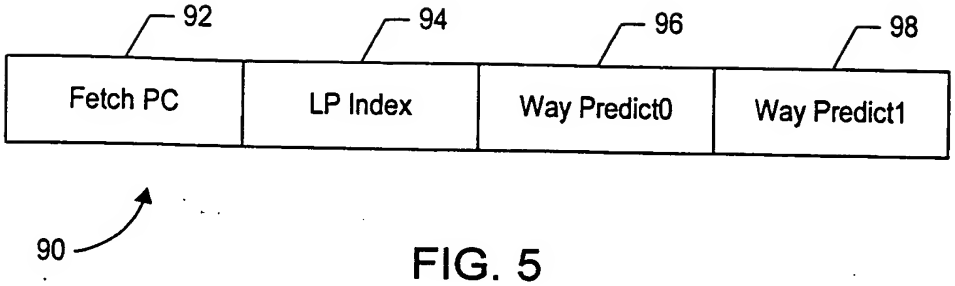

FIG. 5

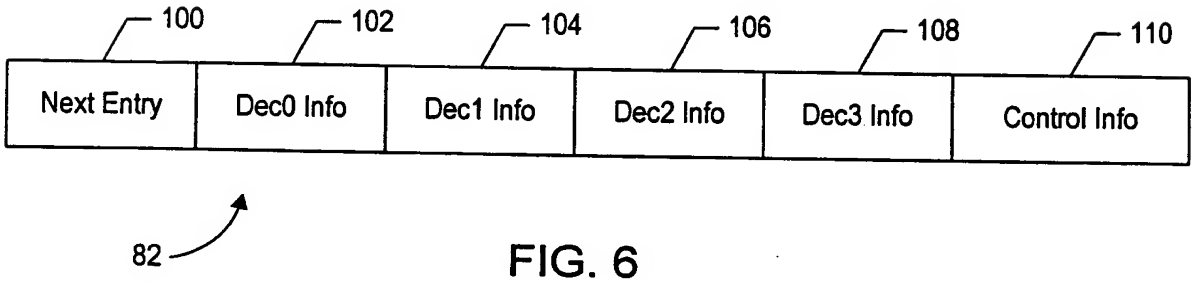

FIG. 6

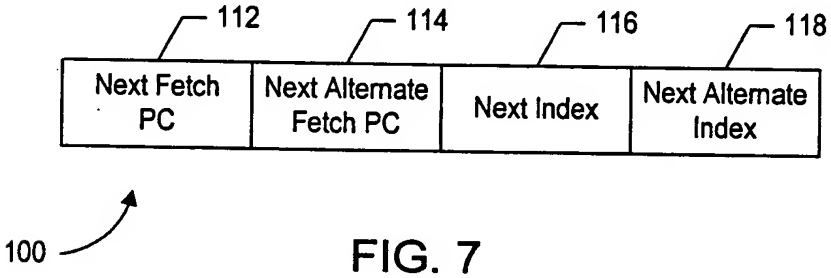

FIG. 7

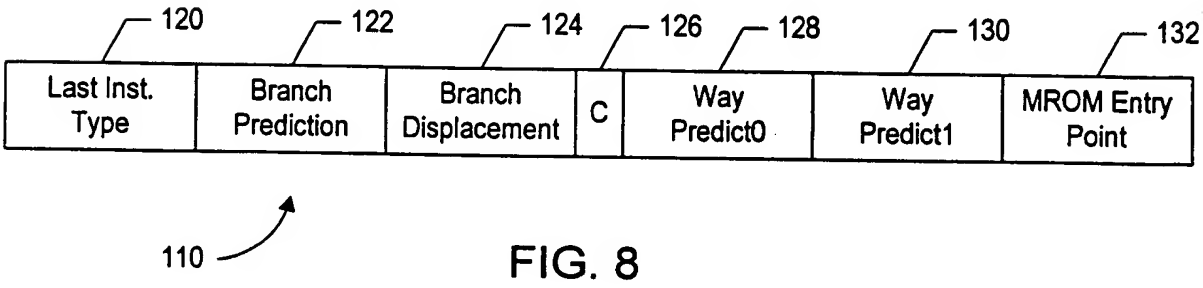

FIG. 8

Line Termination Conditions
Microcode Instruction
Branch Instruction
Maximum # of Instructions
Maximum # of Instruction Bytes
Maximum # of ROPs
Page Crossing
Maximum Number of Destination Registers (Maximum Number of Renames)

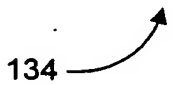

FIG. 9

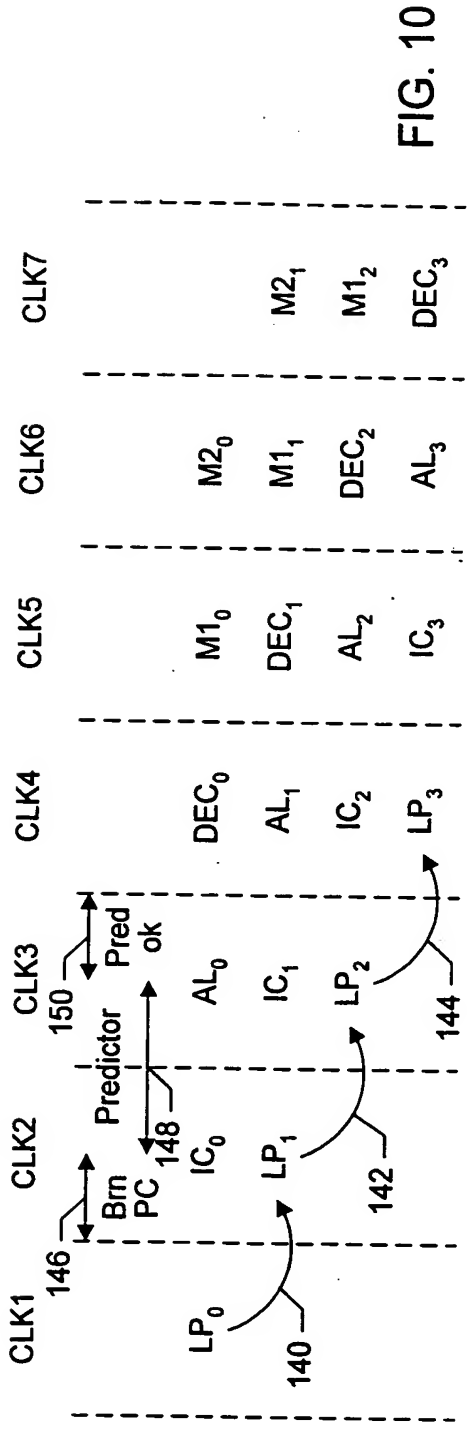
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
146
Brn PC
Predictor
148
Pred ok
150
LP0
IC0
AL0
DEC0
M10
M20
LP1
IC1
AL1
DEC1
M11
M21
140
142
LP2
IC2
AL2
DEC2
M12
144
LP3
IC3
AL3
DEC3

FIG. 10

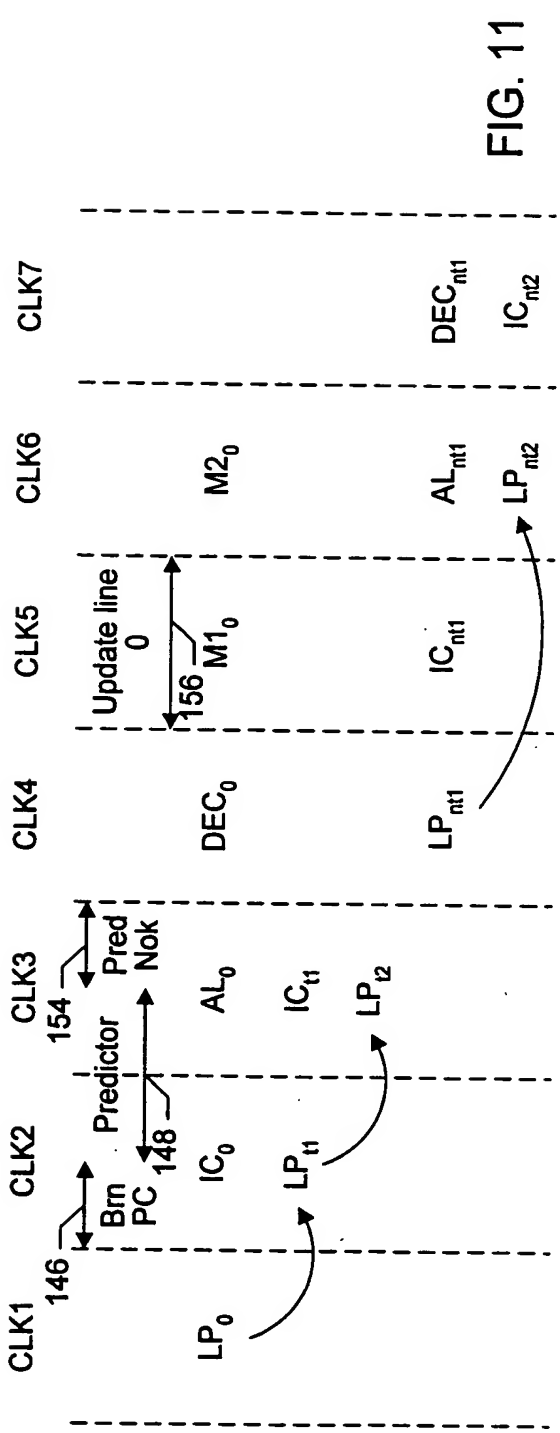
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
146
Brn PC
Predictor
148
154
Pred Nok
Update line 0
156
LP0
IC0
AL0
DEC0
M10
M20
LPt1
ICt1
LPt2
LPnt1
ICnt1
ALnt1
LPnt2
DECnt1
ICnt2

FIG. 11

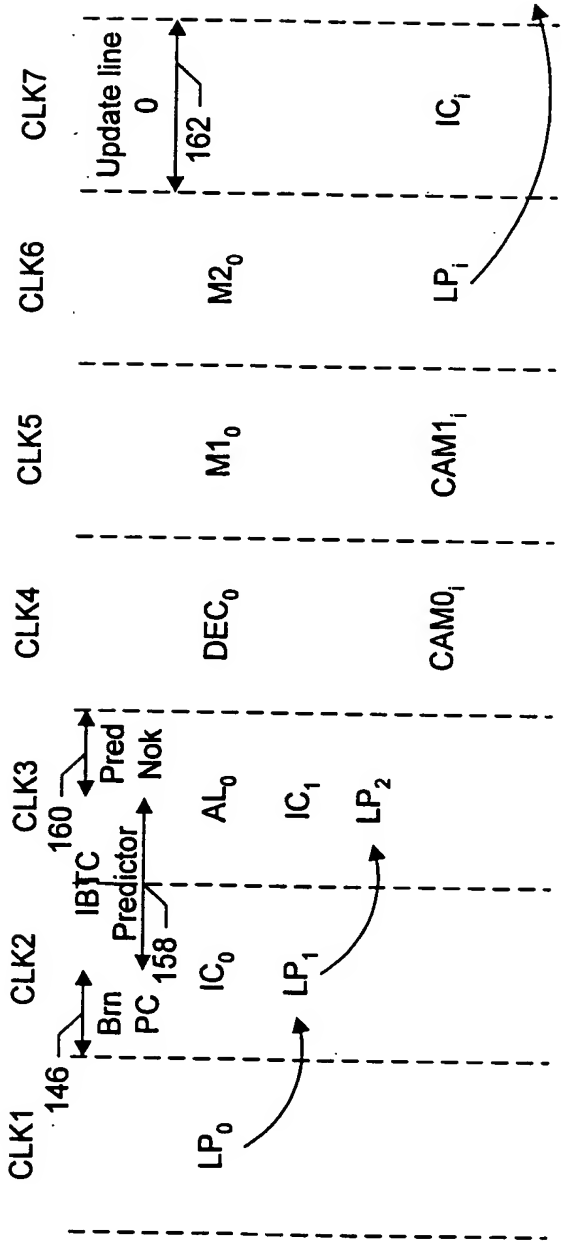
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
146
Brn PC
158
IBTC Predictor
160
Pred Nok
162
Update line 0
LP0
IC0
AL0
DEC0
M10
M20
LP1
IC1
LP2
CAM0i
CAM1i
ICi
LPi

FIG. 12

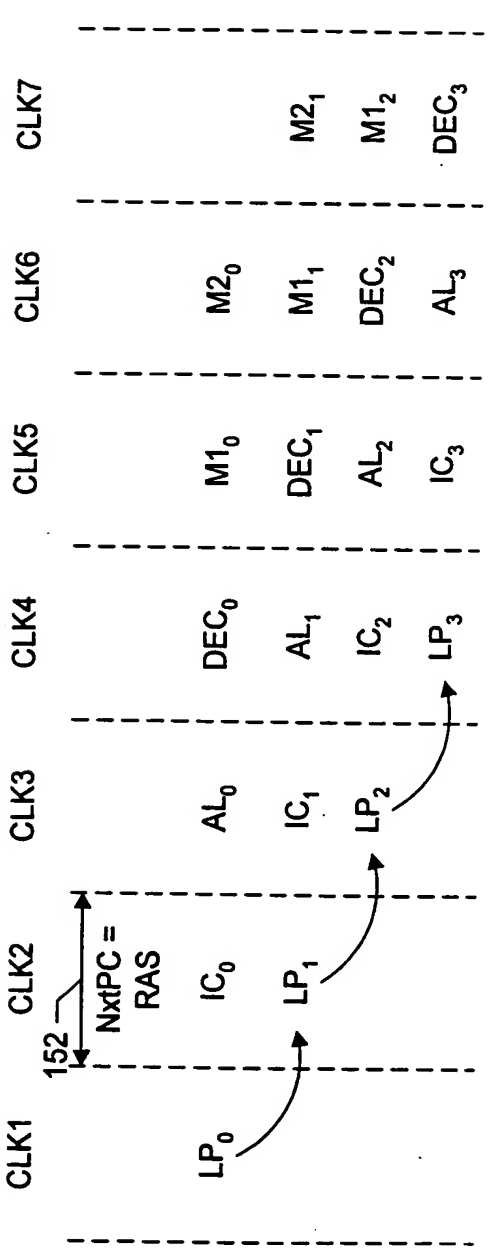
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
152
NxtPC = RAS
LP0
IC0
AL0
DEC0
M10
M20
LP1
IC1
AL1
DEC1
M11
LP2
IC2
AL2
DEC2
M12
LP3
IC3
AL3
DEC3
M21

FIG. 13

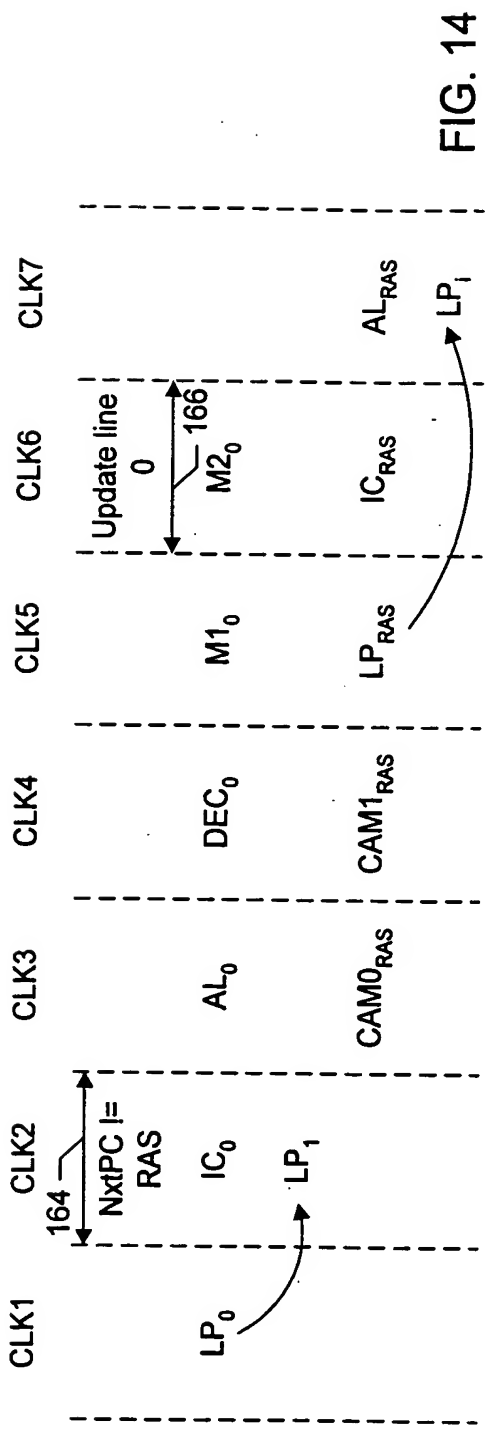
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
164
NxtPC I= RAS
LP0
IC0
LP1
AL0
CAM0RAS
DEC0
CAM1RAS
M10
LPRAS
Update line 0
166
M20
ICRAS
ALRAS
LPi

FIG. 14

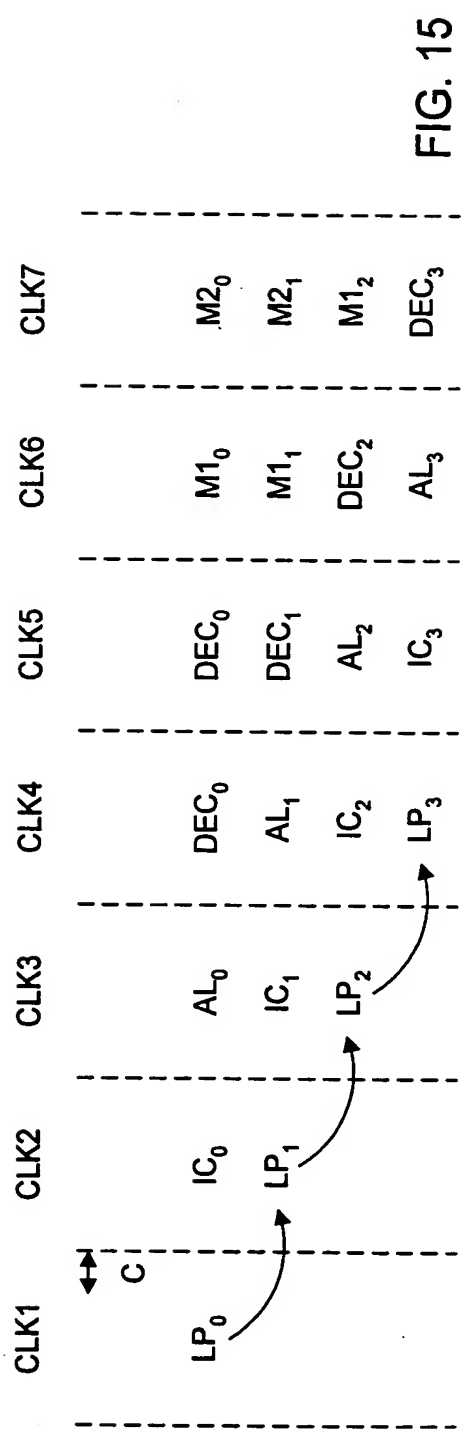
CLK1
CLK2
CLK3
CLK4
CLK5
CLK6
CLK7
C
LP0
IC0
LP1
AL0
IC1
LP2
DEC0
AL1
IC2
LP3
DEC0
DEC1
AL2
IC3
M10
M11
DEC2
AL3
M20
M21
M12
DEC3

FIG. 15

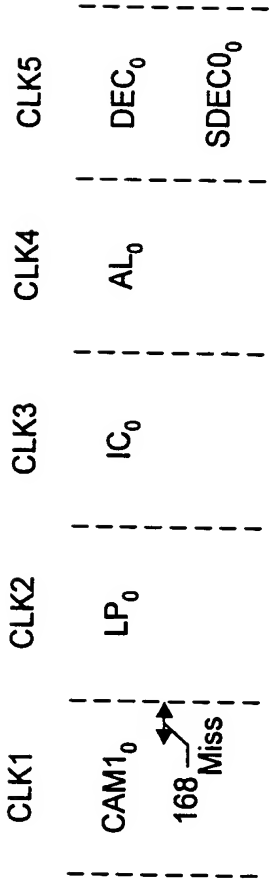

FIG. 16

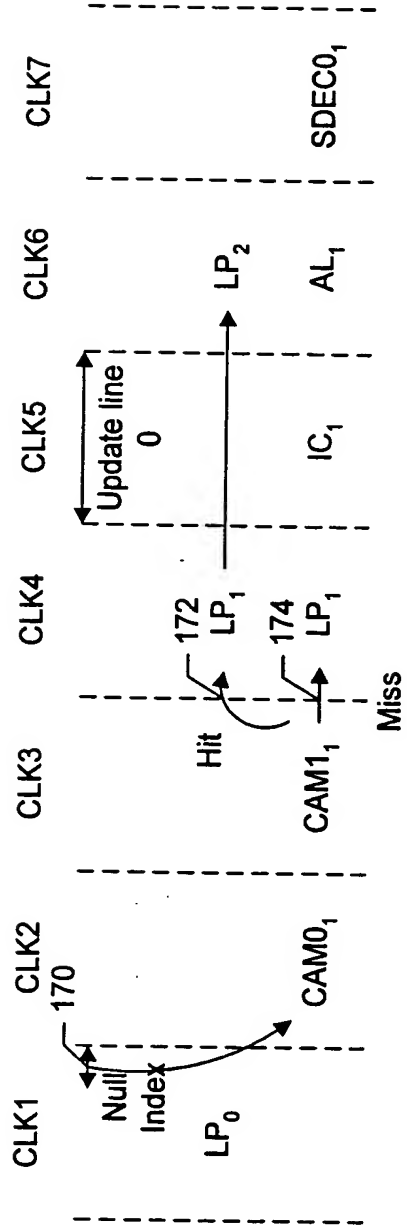

FIG. 17

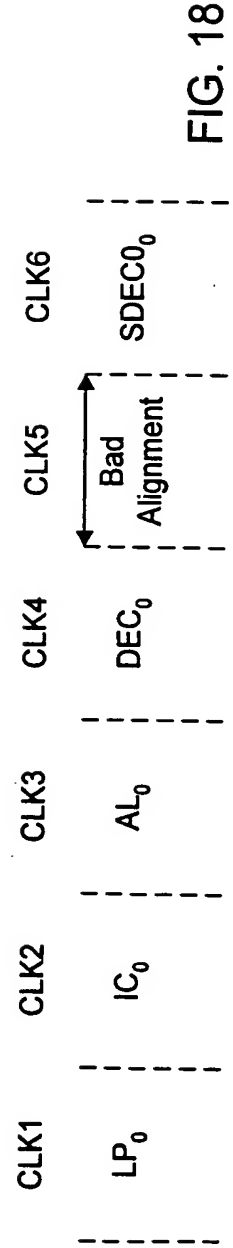

FIG. 18

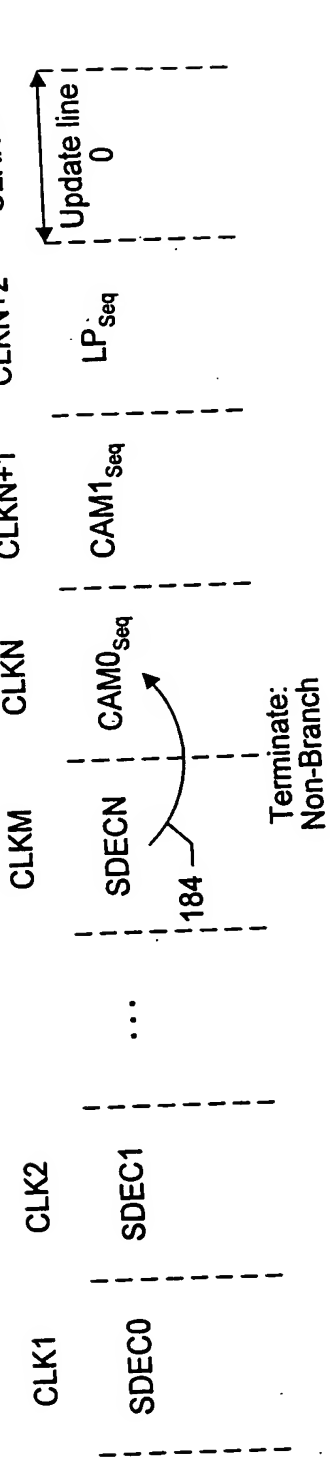
CLK1
CLK2
CLKM
CLKN
CLKN+1
CLKN+2
CLKN+3
SDEC0
SDEC1
SDECN
CAM0Seq
CAM1Seq
LPSeq
Update line 0
184
Terminate: Non-Branch

FIG. 19

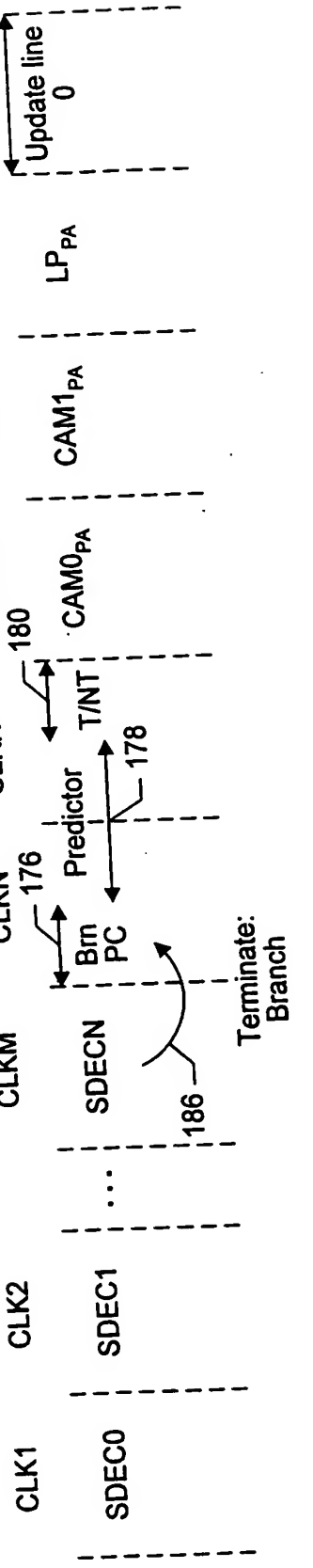
CLK1
CLK2
CLKM
CLKN
CLKN+1
CLKN+2
CLKN+3
CLKN+4
CLKN+5
SDEC0
SDEC1
SDECN
CAM0PA
CAM1PA
LPPA
Update line 0
180
T/NT
178
Predictor
176
Brn PC
186
Terminate: Branch

FIG. 20

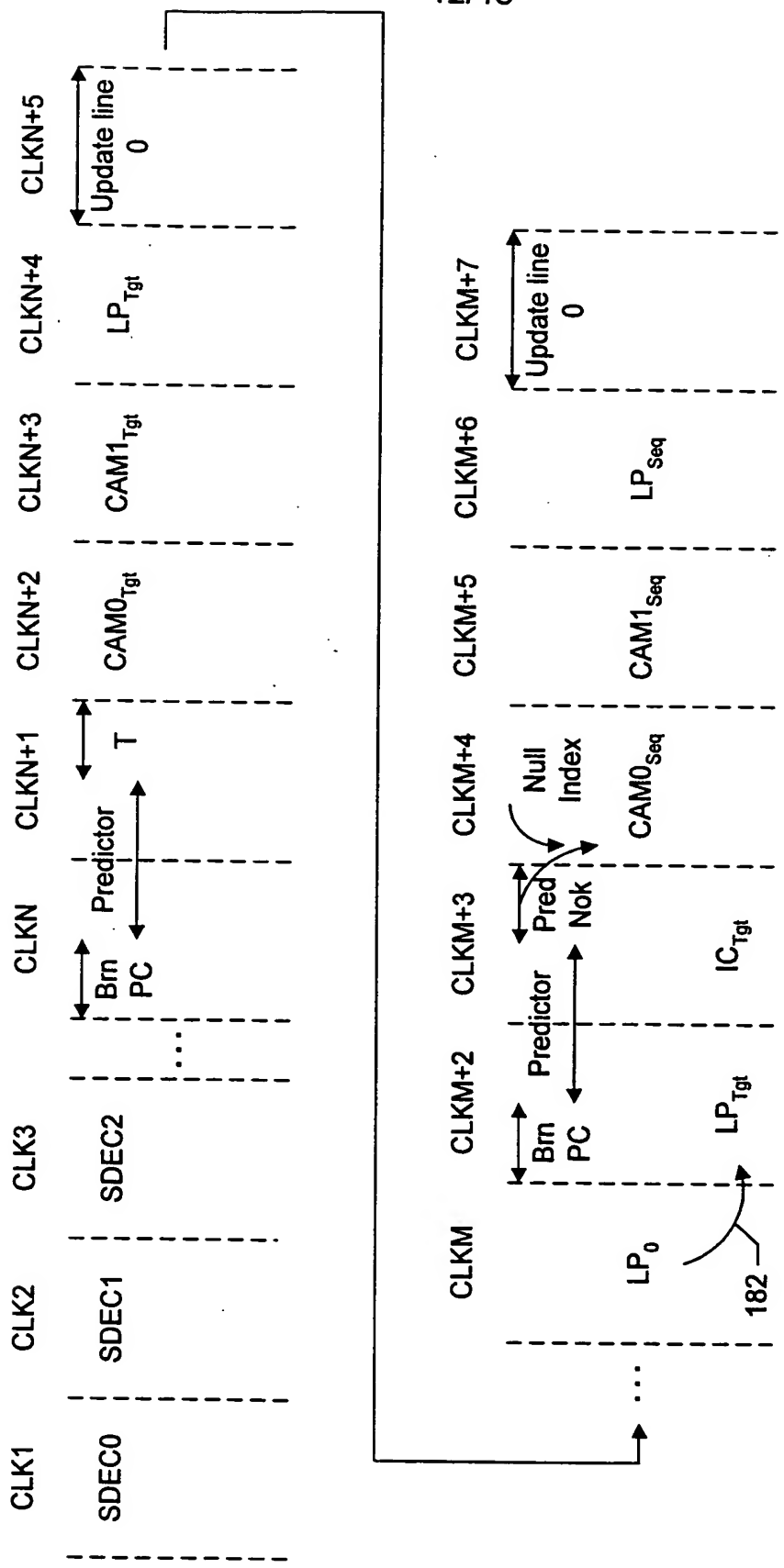
CLK1
CLK2
CLK3
CLKN
CLKN+1
CLKN+2
CLKN+3
CLKN+4
CLKN+5
SDEC0
SDEC1
SDEC2
Brn PC
Predictor
T
$CAM0_{Tgt}$
$CAM1_{Tgt}$
LP_{Tgt}
Update line 0
CLKM
CLKM+2
CLKM+3
CLKM+4
CLKM+5
CLKM+6
CLKM+7
LP_0
182
LP_{Tgt}
IC_{Tgt}
Pred
Nok
Null Index
$CAM0_{Seq}$
$CAM1_{Seq}$
LP_{Seq}

FIG. 21

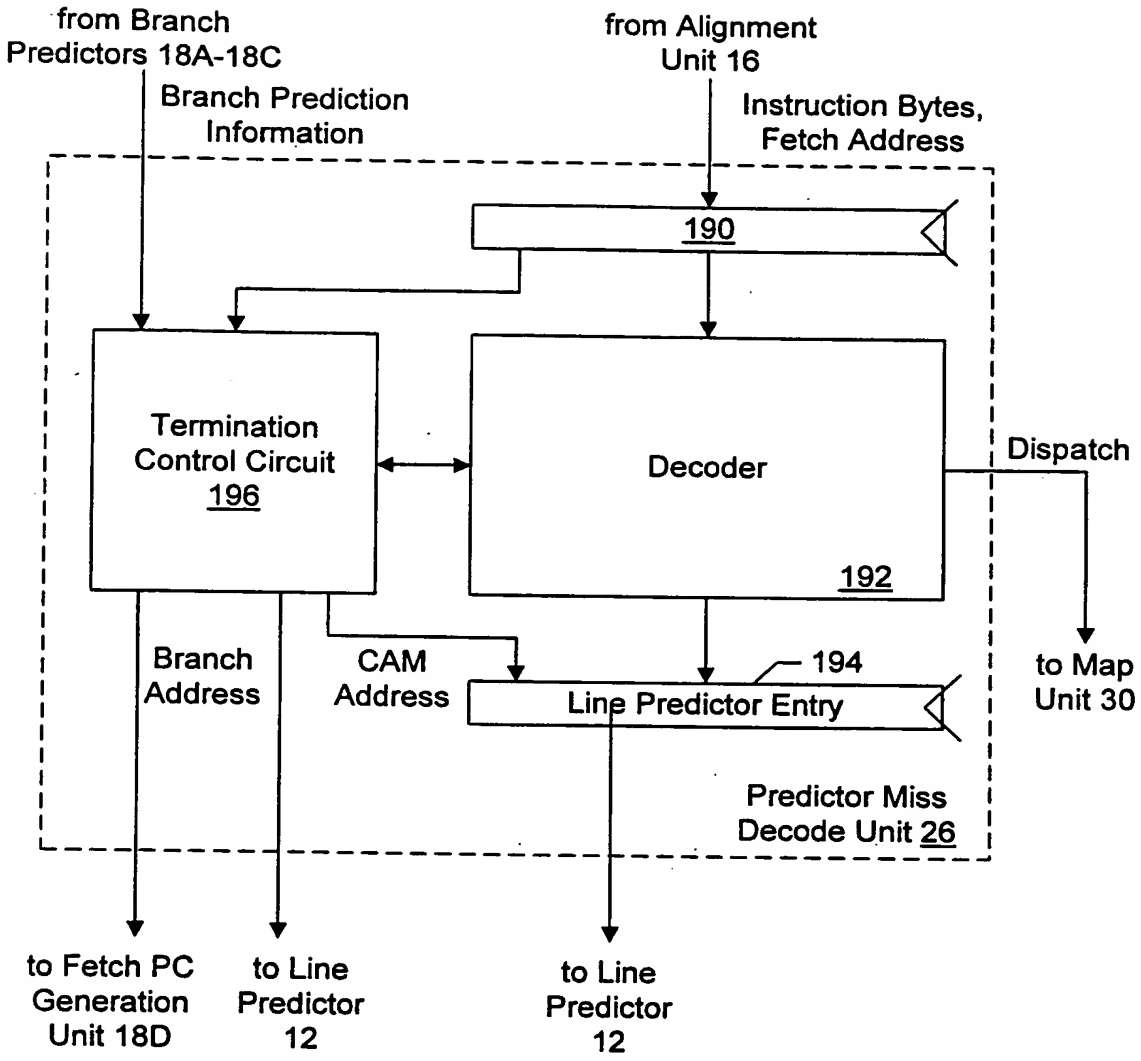
from Branch Predictors 18A-18C
Branch Prediction Information
from Alignment Unit 16
Instruction Bytes, Fetch Address
190
Termination Control Circuit 196
Decoder
192
Dispatch
to Map Unit 30
Branch Address
CAM Address
194
Line Predictor Entry
Predictor Miss Decode Unit 26
to Fetch PC Generation Unit 18D
to Line Predictor 12
to Line Predictor 12

FIG. 22

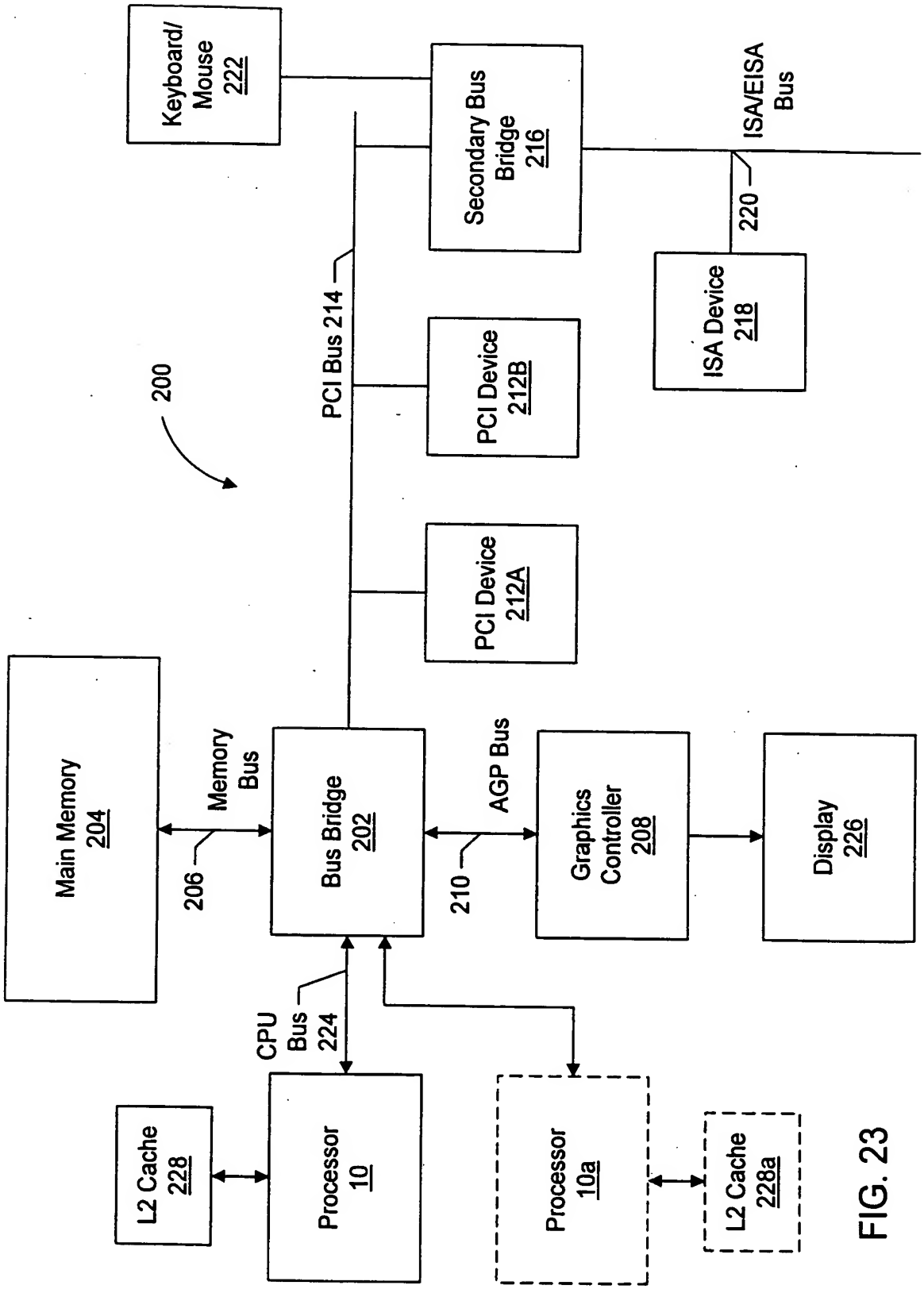
Keyboard/ Mouse 222
Secondary Bus Bridge 216
ISA/EISA Bus
220
ISA Device 218
PCI Bus 214
PCI Device 212B
PCI Device 212A
200
Main Memory 204
Memory Bus
206
Bus Bridge 202
AGP Bus
210
Graphics Controller 208
Display 226
CPU Bus 224
L2 Cache 228
Processor 10
Processor 10a
L2 Cache 228a

FIG. 23

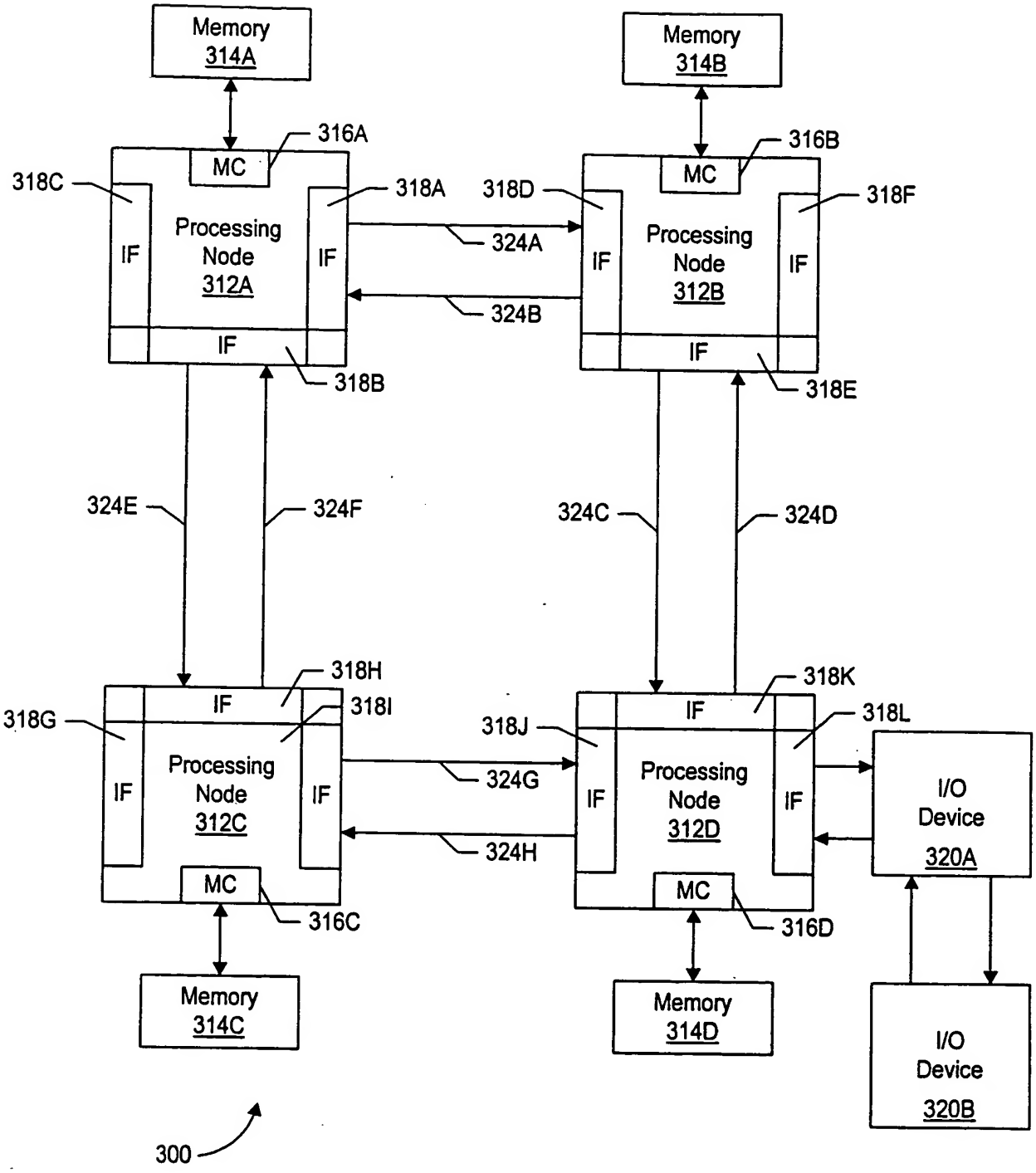
Memory
314A
Memory
314B
316A
316B
MC
MC
318C
318A
318D
318F
IF
Processing
Node
312A
IF
IF
Processing
Node
312B
IF
324A
324B
IF
IF
318B
318E
324E
324F
324C
324D
318H
318K
318G
IF
318I
318J
IF
318L
IF
Processing
Node
312C
IF
324G
IF
Processing
Node
312D
IF
I/O
Device
320A
324H
MC
MC
316C
316D
Memory
314C
Memory
314D
I/O
Device
320B
300

FIG. 24